Claims as Amended

According to First supplemental amendment.

1. (previously presented) A method for reducing light reflectance from via sidewalls in a photolithographic trench patterning dual damascene process comprising the steps of:

providing an inter-metal dielectric (IMD) layer comprising at least one via opening extending through a thickness thereof;

forming an antireflectance coating (ARC) layer over the IMD layer such that the ARC layer is formed over sidewalls of the at least one via opening without filling the at least one via opening; and,

depositing a photoresist layer over the IMD layer and photolithographically patterning a trench opening over the at least one via opening.

2. (previously presented) The method according to claim 1, wherein an etching stop layer is provided over said IMD layer.

3. (previously presented) The method of claim 2, wherein the etching stop layer is selected from the group consisting of silicon oxynitride and silicon nitride.

4. - 6. (cancelled)

7. (previously presented) The method of claim 1, wherein the ARC layer is selected from the group consisting of silicon oxynitride and titanium nitride.

8. (original) The method of claim 1, wherein the ARC layer is formed within a range of thickness from about 100 Angstroms to about 1000 Angstroms.

9. (cancelled)

10. (previously presented) The method of claim 1, wherein the at least one via opening includes at least two via openings formed substantially adjacent to one another.

11. (previously presented) A method of reducing photoresist undercutting due to via sidewall light reflections in a dual damascene trench patterning process comprising the steps of:

providing an inter-metal dielectric (IMD) layer comprising a first anti-reflectance coating (ARC) layer over the IMD layer;

forming a via opening extending through a thickness portion of the IMD layer;

substantially conformally depositing a second ARC layer over said IMD layer and the via openings to cover the via opening sidewalls without filling the via openings; and,

forming a photoresist layer over the IMD layer and photolithographically patterning trench openings disposed at least partially over the via opening and,

forming a photoresist layer over the IMD layer and photolithographically patterning trench openings disposed at least partially over the via opening.

12. (cancelled)

13. (previously presented) The method of claim 11, wherein an etching stop layer is provided over the IMD layer underlying the first ARC layer.

14. (previously presented) The method of claim 13, wherein the etching stop layer is selected from the group consisting of silicon oxynitride and silicon nitride.

15. (previously presented) The method of claim 11, wherein the first and second ARC layers are selected from the group consisting of silicon oxynitride and titanium nitride.

16. (cancelled)

17. (previously presented) The method of claim 11, wherein the second ARC layer is formed within a range of thickness from about 100 Angstroms to about 1000 Angstroms.

18. (previously presented) The method of claim 11, further comprising a second via opening formed substantially adjacent to the via opening.

19. (original) The method of claim 11, further comprising repeating said method as part of a manufacturing process to form a multi-level interconnected semiconductor structure.

20. (previously presented) An improved method of reducing light reflectance from via sidewalls in a dual damascene trench patterning process comprising the steps of:

forming a first dielectric layer over an underlying substrate;

forming at least one second dielectric layer over said first dielectric layer;

forming at least one anti-reflectance coating (ARC) layer over the at least one dielectric layer;

forming at least one via opening through a thickness of the ARC layer, the at least one second dielectric layer, and the first dielectric layer;

forming at least one additional ARC layer substantially conformally over the at least one ARC layer and the at least one via opening to cover the at least one via opening without filling the at least one via opening;

forming a layer of photoresist over the at least one additional ARC layer; and,

photolithographically patterning a trench opening over the at least one via opening.

21. (previously presented) The method of claim 1, wherein the ARC layer is deposited according to a plasma enhanced chemical vapor deposition (PECVD) process.

22. (previously presented) The method of claim 11, wherein at least the second ARC layer is deposited according to a plasma enhanced chemical vapor deposition (PECVD) process.

23. (previously presented) The method of claim 1, wherein the ARC layer consists essentially of silicon oxynitride.

24. (previously presented) The method of claim 11, wherein the first and second ARC layers consist essentially of silicon oxynitride.

25. - 26. (cancelled)